

## 动态近场通信 (NFC) 接口应答机

### 特性

- **NFC 标签类型 4**
- **ISO14443B 兼容 13.56MHz 射频 (RF) 接口支持高达 848kbps 的数据速率**
- **串行外设接口或 I<sup>2</sup>C 接口将近场通信数据交换格式 (NDEF) 消息写入内部 SRAM，并从内部 SRAM 中**
- **读取此消息**
- **用于 NDEF 消息的 3kB SRAM**
- **NDEF 结构的自动校验**
- **中断寄存器和输出引脚以表示 NDEF 读取或写入完成**

### 说明

德州仪器 (TI) 动态 NFC 接口应答机 RF430CL330H 是一个 NFC 标签类型 4 器件，此器件将一个无线 NFC 接口和一个接线 SPI 或 I<sup>2</sup>C 接口组合在一起，将此器件与一个主机相连。SRAM 内的 NDEF 消息可由集成型 SPI 或 I<sup>2</sup>C 串行通信接口写入和读取，而此消息也可通过集成型 ISO14443B 兼容 RF 接口（支持高达 848kbps 数据速率）进行无线存取和更新。

这可实现针对替代载波的 NFC 连接切换，如同 *Bluetooth™*，*Bluetooth*低功耗 (BLE)，和 Wi-Fi 等，只需一次敲击的简便且直观的配对过程或认证过程。作为一个常见 NFC 接口，RF430CL330H 使得终端设备能够与启用 NFC 的智能手机、平板电脑和笔记本电脑的快速增长的基础设施进行通信。

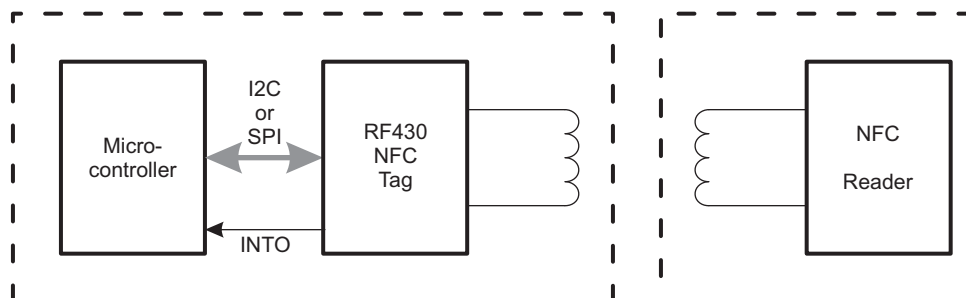


图 1. 典型应用

表 1. 订购信息<sup>(1)</sup>

T <sub>A</sub>	封装的器件 <sup>(2)</sup>
	塑料 14 引脚薄型小尺寸封装 (TSSOP) (PW)
-40°C 至 85°C	RF430CL330HCPWR

- (1) 要获得最新的封装和订购信息，请参阅本文档末尾的封装选项附录，或者浏览 TI 网站[www.ti.com](http://www.ti.com)。
- (2) 封装图示，标准包装数量，散热数据，符号以及 PCB 设计指南可从[www.ti.com/packaging](http://www.ti.com/packaging)上获得。

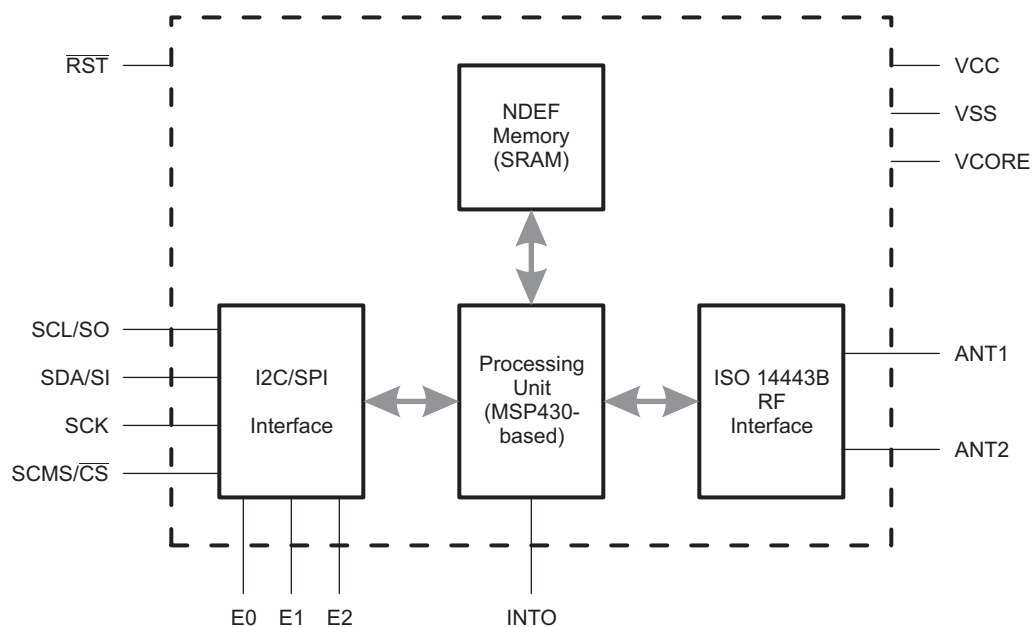
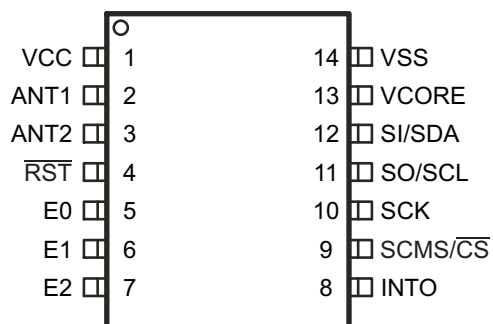


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**Functional Block Diagram****PW PACKAGE  
(TOP VIEW)**

**Table 2. Terminal Functions**

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
VCC	1	PWR	3.3-V power supply
ANT1	2	RF	Antenna input 1
ANT2	3	RF	Antenna input 2
$\overline{\text{RST}}$	4	I	Reset input (active low) <sup>(2)</sup>
E0 (TMS)	5	I	I2C address select 0 SPI mode select 0 (JTAG test mode select <sup>(3)</sup> )
E1 (TDO)	6	I (O)	I2C address select 1 SPI mode select 1 (JTAG test data output <sup>(3)</sup> )
E2 (TDI)	7	I	I2C address select 2 <sup>(4)</sup> (JTAG test data in <sup>(3)</sup> )
INTO (TCK)	8	O	Interrupt output (JTAG test clock <sup>(3)</sup> )
SCMS/ $\overline{\text{CS}}$	9	I	Serial Communication Mode Select (during device initialization) <sup>(5)</sup> Chip select (in SPI mode)
SCK	10	I	SPI clock input (SPI mode)
SO/SCL	11	I/O	SPI slave out (SPI mode) I2C clock (I2C mode)
SI/SDA	12	I/O	SPI slave in (SPI mode) I2C data (I2C mode)
VCORE	13	PWR	Regulated core supply voltage
VSS	14	PWR	Ground supply

(1) I = Input, O = Output, PWR = Power, RF = RF Antenna

(2) With integrated pullup.

(3) This device does not provide JTAG-compliant boundary scan test.

(4) Tie low in SPI mode to avoid floating inputs.

(5) Selects I2C or SPI mode during power-up and initialization (see and ). Tie SCMS/ $\overline{\text{CS}}$  low to select I2C mode.

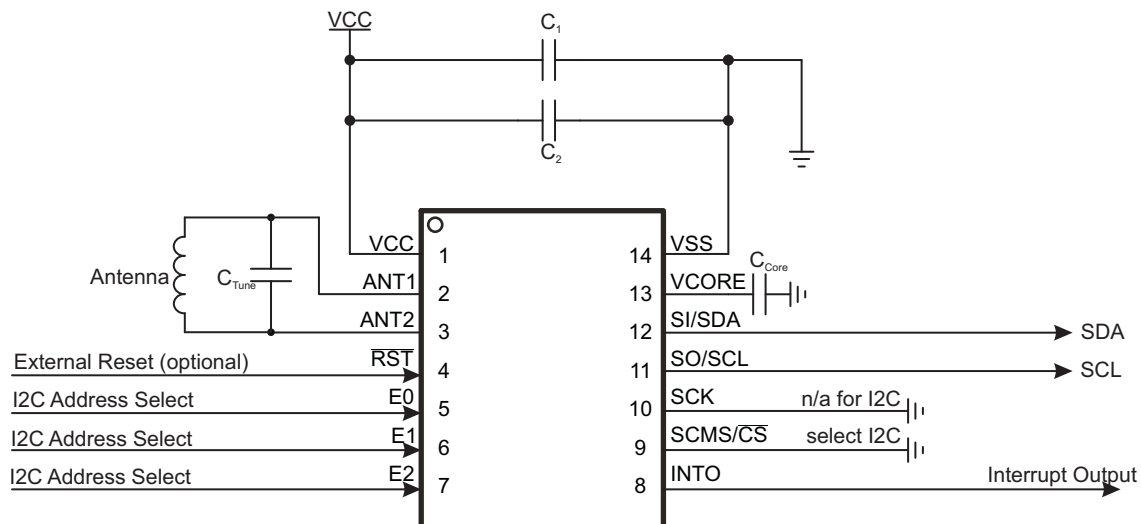


Figure 2. Example Application Diagram (I2C Operation)

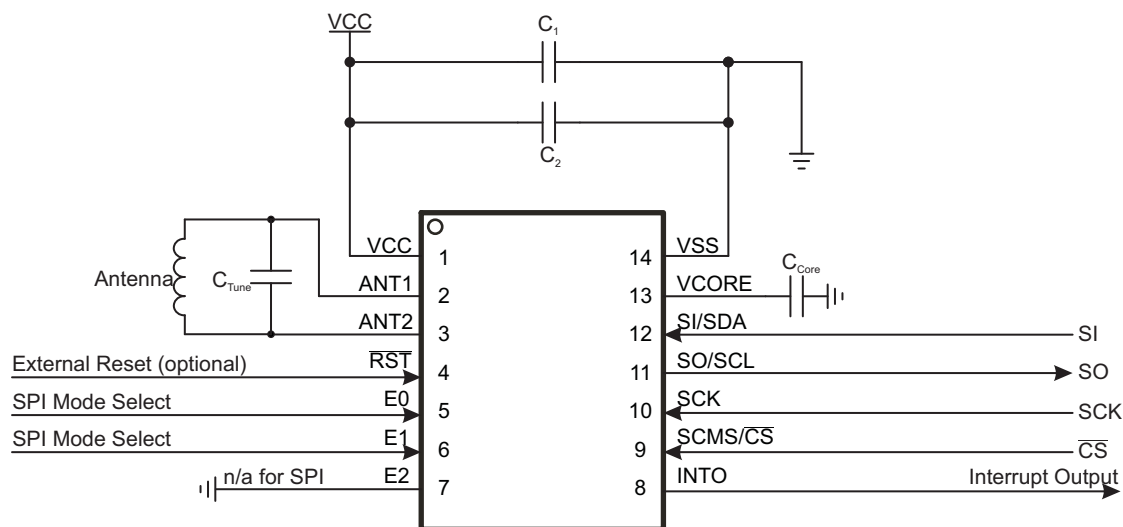


Figure 3. Example Application Diagram (SPI Operation)

## Detailed Description

### Serial Communication Interface

A "dual-mode" serial communication interface supports either SPI or I2C communication. The serial interface allows writing and reading the internal NDEF message memory as well as configuring the device operation.

### SPI or I2C Mode Selection

The selection between I2C or SPI mode takes place during the power-up and initialization phase of the device based on the input level at pin SCMS/ $\overline{\text{CS}}$  (see [Table 3](#)).

**Table 3. SPI or I2C Mode Selection**

Input Level at SCMS/ $\overline{\text{CS}}$ During Initialization	Selected Serial Interface
0	I2C
1	SPI

During initialization, an integrated pullup resistor pulls SCMS/ $\overline{\text{CS}}$  high, which makes SPI the default interface. To enable I2C, this pin must be tied low externally. The pullup resistor is disabled after initialization to avoid any current through the resistor during normal operation. In SPI mode, the pin reverts to its  $\overline{\text{CS}}$  functionality after initialization.

### Communication Protocol

The tag is programmed and controlled by writing data into and reading data from the address map shown in [Table 4](#) via the serial interface (SPI or I2C).

**Table 4. User Address Map**

Range	Address	Size	Description
Registers	0xFFFFE	2B	Control Register
	0xFFFFC	2B	Status Register
	0xFFFFA	2B	Interrupt Enable
	0xFFFF8	2B	Interrupt Flags
	0xFFFF6	2B	CRC Result (16-bit CCITT)
	0xFFFF4	2B	CRC Length
	0xFFFF2	2B	CRC Start Address
	0xFFFF0	2B	Communication Watchdog Control Register
	0xFFEE	2B	Version
	0xFFEC	2B	Reserved
	0xFFEA	2B	Reserved
	0xFFE8	2B	Reserved
	0xFFE6	2B	Reserved
	0xFFE4	2B	Reserved
	0xFFE2	2B	Reserved
	0xFFE0	2B	Reserved
Reserved	0x4000 to 0xFFDF		Reserved
	0x0C00 to 0x3FFF	13kB	Reserved (for example, future extension of NDEF Application Memory size)
NDEF	0x0000 to 0x0BFF	3kB	NDEF Application Memory

### NOTE

#### Crossing Range Boundaries

Crossing range boundaries causes writes to be ignored and reads to return undefined data.

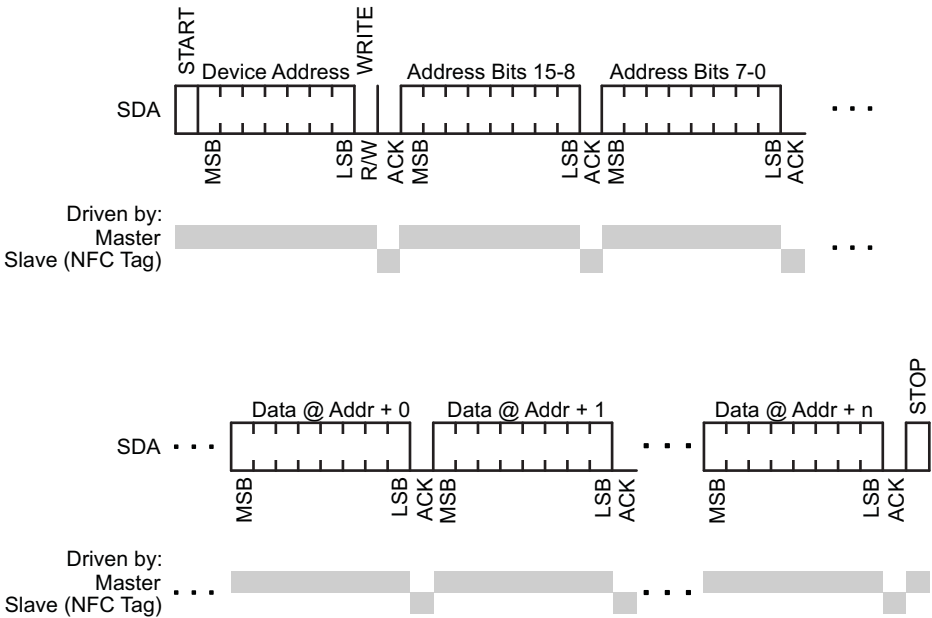
**I2C Protocol**

A command is always initiated by the master by addressing the device using the specified I2C device address. The device address is a 7-bit I2C address. The upper four bits are hard-coded, and the lower three bits are programmable by the input pins E0 through E2.

**Table 5. I2C Device Address**

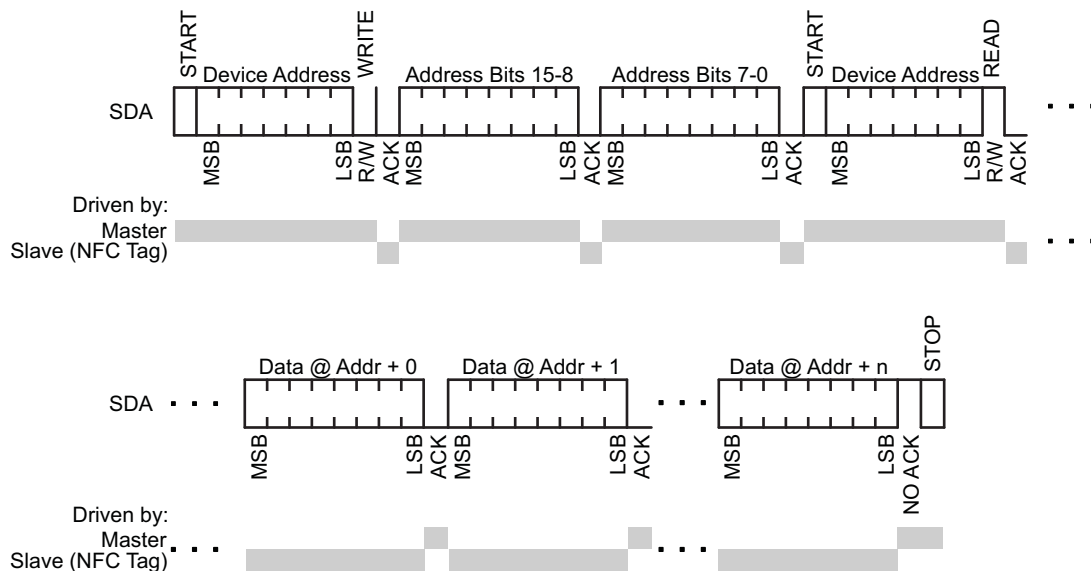
Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	E2	E1	E0
MSB				LSB		

To write data, the device is addressed using the specified I2C device address with  $R/\overline{W} = 0$ , followed by the upper 8 bits of the first address to be written and the lower 8 bits of that address. Next (without a repeated start), the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by the STOP condition on the I2C bus.



**Figure 4. I2C Write Access**

To read data, the device is addressed using the specified I2C device address with  $R/\overline{W} = 0$ , followed by the upper 8 bits of the first address to be written and then the lower 8 bits of that address. Next, a repeated start condition is expected with the I2C device address and  $R/\overline{W} = 1$ . The device then transmit data starting at the specified address until a non-acknowledgment and a STOP condition is received.



**Figure 5. I2C Read Access**

### BIP-8 Communication Mode With I2C

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

**Table 6. Write Access**

Master	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
Slave	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the I2C device address).

**Table 7. Read Access**

Master	Address Bits 15 to 8	Address Bits 7 to 0	n/a	n/a	n/a
Slave	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access, the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address and the 2 transmitted data bytes, and it is transmitted back to the master. The BIP-8 does not include the device address.

## SPI Protocol

The SPI communication mode (SCK idle state and clock phase) is selected by tying E0 and E1 to VSS or VCC according to [Table 8](#).

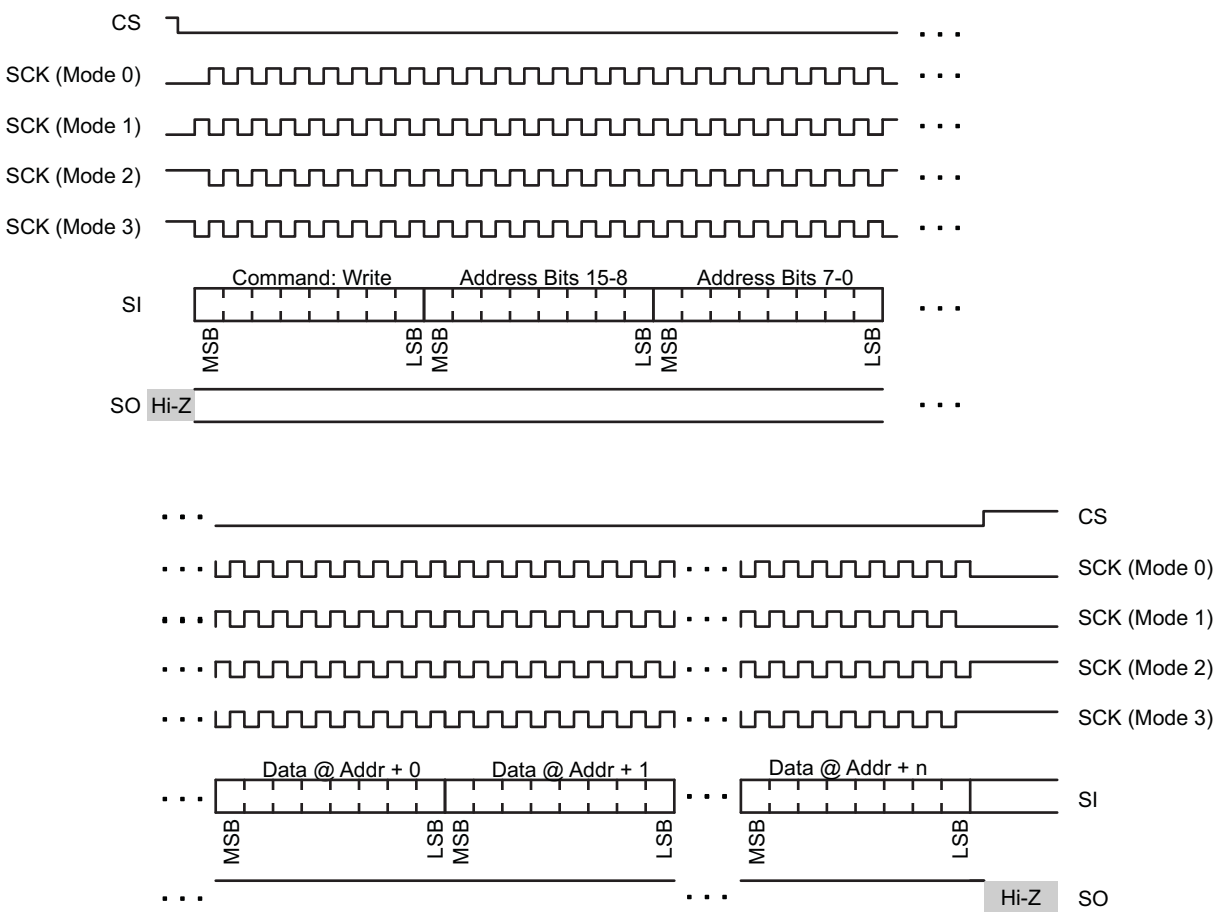
**Table 8. SPI Mode Selection**

E1	E0	SPI Mode
0	0	<b>SPI Mode 0</b> with CPOL = 0 and CPHA = 0 SCK idle state: 0 SI capture starts on the first edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.
0	1	<b>SPI Mode 1</b> with CPOL = 0 and CPHA = 1 SCK idle state: 0 SI capture starts on the second edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	0	<b>SPI Mode 2</b> with CPOL = 1 and CPHA = 0 SCK idle state: 1 SI capture starts on the first edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	1	<b>SPI Mode 3</b> with CPOL = 1 and CPHA = 1 SCK idle state: 1 SI capture starts on the second edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.

An SPI communication is always initiated by the master by pulling the  $\overline{\text{CS}}$  pin low.

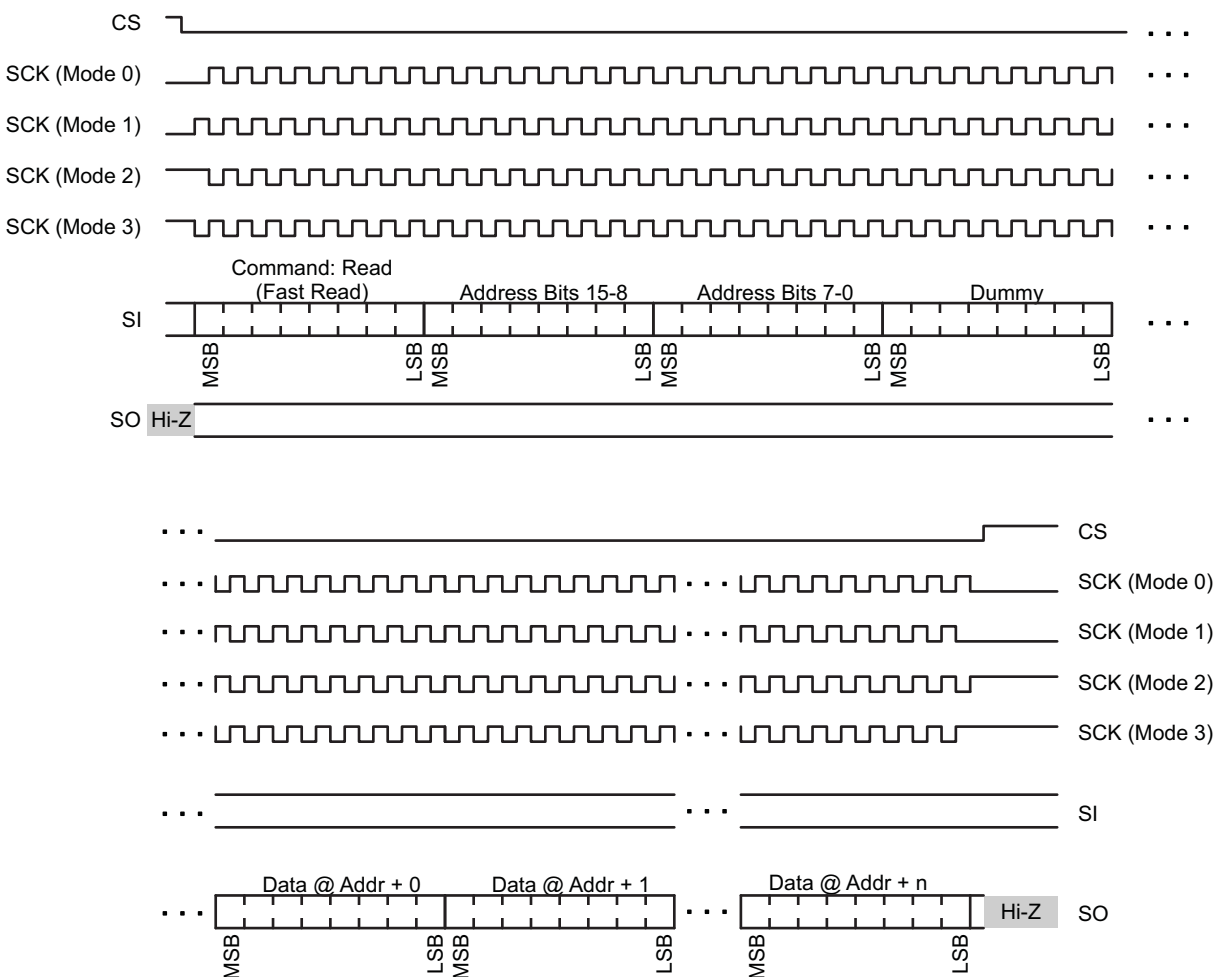
To write data into the device, this is followed by the master sending a write command (0x02) followed by the upper 8 bits of the first address to be written and then the lower 8 bits of that address. Next, the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by pulling the  $\overline{\text{CS}}$  pin high.





**Figure 6. SPI Write Access**

To read data from the device, pulling the  $\overline{\text{CS}}$  pin low is followed by the master sending a read command (0x03 or 0x0B) followed by the upper 8 bits of the first address to be written, the lower 8 bits of that address and a dummy byte. The device responds with the data that is read starting at the specified address until the  $\overline{\text{CS}}$  pin is pulled high.



**Figure 7. SPI Read Access (Command: 0x03 or 0x0B)**

Commands other than write (0x02) and read (0x03 or 0x0B) are ignored. There is no difference in using the read command 0x03 or 0x0B.

### BIP-8 Communication Mode With SPI

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

**Table 9. Write Access**

SI	Command: Write	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
SO	n/a	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the write-command byte.)

**Table 10. Read Access**

SI	Command: Read	Address Bits 15 to 8	Address Bits 7 to 0	Dummy Byte	n/a	n/a	n/a
SO	n/a	n/a	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address, the received dummy byte and the 2 transmitted data bytes and transmitted back to the master. It does not include the read-command byte.

## Registers

### NOTE

#### Endianness

All 16-bit registers are little-endian: the least significant byte with bits 7-0 is at the lowest address (and this address is always even). The most significant byte with bits 15-8 is at the highest address (always odd).

## General Control Register

**Table 11. General Control Register**

Addr:	15	14	13	12	11	10	9	8
0xFFFF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFFE	Reserved	Standby Enable	BIP-8	INTO Drive	INTO High	Enable INT	Enable RF	SW-Reset

**Table 12. General Control Register Description**

Bit	Field	Type	Reset	Description
0	SW-Reset	W	0	0b = Always reads 0. 1b = Resets the device to default settings and clears memory. The serial communication is restored after $t_{Ready}$ , and the register settings and NDEF data memory must be restored afterward.
1	Enable RF	R/W	0	Global enable of RF interface. The RF interface should be disabled when writing to the NDEF application memory. Enabling the RF interface triggers a basic check of the NDEF structure. If this check fails, the RF interface remains disabled and the NDEF Error interrupt flag is set. When the RF interface is enabled, writes using the serial interface (except to disable the RF interface) are discouraged to avoid any interference with RF communication. 0b = RF interface disabled 1b = RF interface enabled
2	Enable INT	R/W	0	Global Interrupt Output Enable 0b = Interrupt output disabled. The INTO pin is Hi-Z. 1b = Interrupt output enabled. The INTO pin signals any enabled interrupt according to the INTO High and INTO Drive bits.
3	INTO High	R/W	0	Interrupt Output pin INTO Configuration 0b = Interrupts are signaled with an active low 1b = Interrupts are signaled with an active high
4	INTO Drive	R/W	0	Interrupt Output pin INTO Configuration 0b = Pin is Hi-Z if there is no pending interrupt. Application provides an external pullup resistor if bit 3 (INTO Active High) = 0. Application provides an external pulldown resistor if bit 3 (INTO Active High) = 1. 1b = Pin is actively driven high or low if there is no pending interrupt. It is driven high if bit 3 (INTO Active High) = 0. It is driven low if bit 3 (INTO Active High) = 1.
5	BIP-8	R/W	0	Enables BIP-8 communication mode (bit interleaved parity). If BIP-8 is enabled, a separate running tally is kept of the parity (that is, the number of ones that occur) for every bit position in the bytes included in the BIP-8 calculation. The corresponding bit position of the BIP-8 byte is set to 1 if the parity is currently odd and is set to 0 if the parity is even – resulting in an overall even parity for each bit position including the BIP-8 byte. All communication when this bit is set must follow the conventions defined in the BIP-8 communication mode sections for <a href="#">I2C</a> and <a href="#">SPI</a> . 0b = BIP-8 communication mode disabled 1b = BIP-8 communication mode enabled

**Table 12. General Control Register Description (continued)**

Bit	Field	Type	Reset	Description
6	Standby Enable	R/W	0	Enables a low-power standby mode. The standby mode is entered if the RF interface is disabled, the communication watchdog is disabled, and no serial communication is ongoing. 0b = Standby mode disabled 1b = Standby mode enabled
7	Reserved	R/W	0	
8-15	Reserved	R	0	

## Status Register

**Table 13. Status Register**

Addr:	15	14	13	12	11	10	9	8
0xFFFD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFFC	Reserved	Reserved	Reserved	Reserved	Reserved	RF Busy	CRC Active	NDEF Ready

**Table 14. Status Register Description**

Bit	Field	Type	Reset	Description
0	Ready	R	0	0b = Device not ready to receive updates to the NDEF memory from the serial interface. 1b = Device ready. NDEF memory can be written by the serial interface.
1	CRC Active	R	0	0b = No CRC calculation ongoing 1b = CRC calculation ongoing
2	RF Busy	R	0	0b = No RF communication ongoing 1b = RF communication ongoing
3-15	Reserved	R	0	

## Interrupt Registers

The interrupt enable register determines what interrupt events are signaled on the external output pin INTO. Setting any bits high in this register allows the corresponding events to trigger the interrupt signal.

All enabled interrupt signals are ORed together and the result is signaled on the output pin INTO.

**Table 15. Interrupt Enable Register**

Addr:	15	14	13	12	11	10	9	8
0xFFFB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFFA	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

**Table 16. Interrupt Enable Register Description**

Bit	Field	Type	Reset	Description
0-15	Interrupt Enables	R/W	0	Enable for the corresponding IRQ. All enabled interrupt signals are ORed together and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled

The interrupt flag register is used to report the status of any interrupts that are pending. Setting any bit high in this register acknowledges and clears the interrupt associated with the respective bit.

**Table 17. Interrupt Flag Register**

Addr:	15	14	13	12	11	10	9	8
0xFF9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFF8	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

**Table 18. Interrupt Flag Register Description**

Bit	Field	Type	Reset	Description
0-15	Interrupt Flags	R/W	0	Flag pending IRQ. Read Access: 0b = No pending IRQ. 1b = Pending IRQ. Write Access: 0b = No change. 1b = Clear pending IRQ flag.

**Table 19. Interrupts**

Bit	Field	Description
0	Reserved	
1	End of Read	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a read of the NDEF message.
2	End of Write	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a write into the NDEF message.
3	CRC Calculation Completed	This IRQ occurs when a CRC calculation that is triggered by writing into the CRC registers is completed and the result can be read from the CRC result register (see <a href="#">CRC Registers</a> ).
4	BIP-8 Error Detected	This IRQ occurs when a BIP-8 error is detected (only if the BIP-8 communication mode is enabled).
5	NDEF Error	This IRQ occurs if an error is detected in the NDEF structure after an attempt to enable the RF interface.
6	Reserved	
7	Generic Error	This IRQ occurs for any error that makes the device unreliable or non-operational.
8-15	Reserved	

## CRC Registers

Writing the CRC address and the CRC length registers initiates a 16-bit CRC calculation of the specified address range. The length is always assumed to be even (16-bit aligned). Writing the length register starts the CRC calculation.

During the CRC calculation, the CRC active bit is set (=1). When the calculation is complete, the "CRC completion" interrupt flag is set and the result of the CRC calculation can be read from the CRC result register. It is recommended to perform a CRC calculation only when the RF interface is disabled (RF Enable = 0).

**Table 20. CRC Result Register**

Addr:	15	14	13	12	11	10	9	8
0xFFF7	CRC CCITT Result (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF6	CRC CCITT Result (low byte)							

**Table 21. CRC Result Register Description**

Bit	Field	Type	Reset	Description
0-15	CRC-CCITT Result	R	0	CRC-CCITT Result

**Table 22. CRC Length Register**

Addr:	15	14	13	12	11	10	9	8
0xFFF5	CRC Length (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF4	CRC Length (low byte)							

**Table 23. CRC Length Register Description**

Bit	Field	Type	Reset	Description
0-15	CRC Length	RW	0	CRC Length - always assumed to be even (Bit 0 = 0). Writing into high byte starts CRC calculation.

**Table 24. CRC Start Address Register**

Addr:	15	14	13	12	11	10	9	8
0xFFF3	CRC Start Address (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF2	CRC Start Address (low byte)							

**Table 25. CRC Start Address Register Description**

Bit	Field	Type	Reset	Description
0-15	CRC Start Address	RW	0	CRC Start Address. Defines start address within NDEF application data memory. This address is always assumed to be even (bit 0 = 0).

The CRC is calculated based on the CCITT polynomial initialized with 0xFFFF.

CCITT polynomial:  $x^{16} + x^{12} + x^5 + 1$

## Communication Watchdog Register

When the communication watchdog is enabled, it expects a write or read access within a specified period; otherwise, the watchdog resets the device. If the BIP-8 communication mode is enabled, the transfer must be valid to be accepted as a watchdog reset.

**Table 26. Communication Watchdog Register**

Addr:	15	14	13	12	11	10	9	8
0xFFF1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFF0	Reserved	Reserved	Reserved	Reserved	Timeout Period Selection			Enable

**Table 27. Communication Watchdog Register Description**

Bit	Field	Type	Reset	Description
0	Enable	R/W	0	0b = Communication Watchdog disabled 1b = Communication Watchdog enabled
1	Timeout Period Selection	R/W	0	000b = 2 s $\pm$ 30% <sup>(1)</sup> 001b = 32 s $\pm$ 30% <sup>(1)</sup> 010b = 8.5 min $\pm$ 30% <sup>(1)</sup> 011b to 111b = Reserved
4-15	Reserved	R	0	

(1) This value is based on use of the integrated low-frequency oscillator with a frequency of 256 kHz  $\pm$  30%.

## Version Registers

Provides version information about the implemented ROM code.

**Table 28. Version Register**

Addr:	15	14	13	12	11	10	9	8
0xFFEF	Software Version							
Addr:	7	6	5	4	3	2	1	0
0xFFEE	Software Identification							

**Table 29. Version Register Description**

Bit	Field	Type	Reset	Description
0-7	Software Identification	R		0x01: RF430CL330H Firmware
8-15	Software Version	R		Software version



## NFC Type-4 Tag Functionality

The device supports an ISO 14443B compliant transponder that operates according to the NFC Forum Tag Type-4 specification and supports the NFC Forum NDEF (NFC Data Exchange Format) requirements. Through the RF interface, the user can read and update the contents in the NDEF data memory. The contents in the NDEF data memory (stored in SRAM) are stored as long as power is maintained.

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### NOTE

This device does not have nonvolatile memory; therefore, the information stored in the NDEF data memory is lost when power is removed.

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This device does not support the peer-to-peer or reader/writer modes in the ISO18092/NFC Forum specification. All RF communication between an NFC forum device and this device is in the passive tag mode. The device responds by load modulation and is not considered an intentional radiator.

This device is intended to be used in applications where the primary reader/writer is an NFC-enabled cell phone. The device enables data transfer to and from an NFC phone by RF to the host application that is enabled with the dual interface device. In this case, the host application can be considered the destination device, and the cell phone or other type of mobile device is treated as the end-point device.

This device supports ISO14443-3, ISO 14443-4, and NFC Forum commands as described in the following sections. A high-level overview of the ISO14443B and NFC commands and responses are shown in [Figure 8](#).

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported.

By default, the device reports only the capability to support 106-kbps, because some cell phones do not work correctly with the information that the device supports higher data rates. To enable higher data rates, a special sequence is required as described in [Data Rate Settings](#).

The ISO14443B command and response structure is detailed in ISO 14443-3, ISO 14443-4, and NFC Forum-TS-Digital Protocol. The applicable ISO 7816-4 commands are detailed in NFC Forum-TS-Type-4-Tag\_2.0.

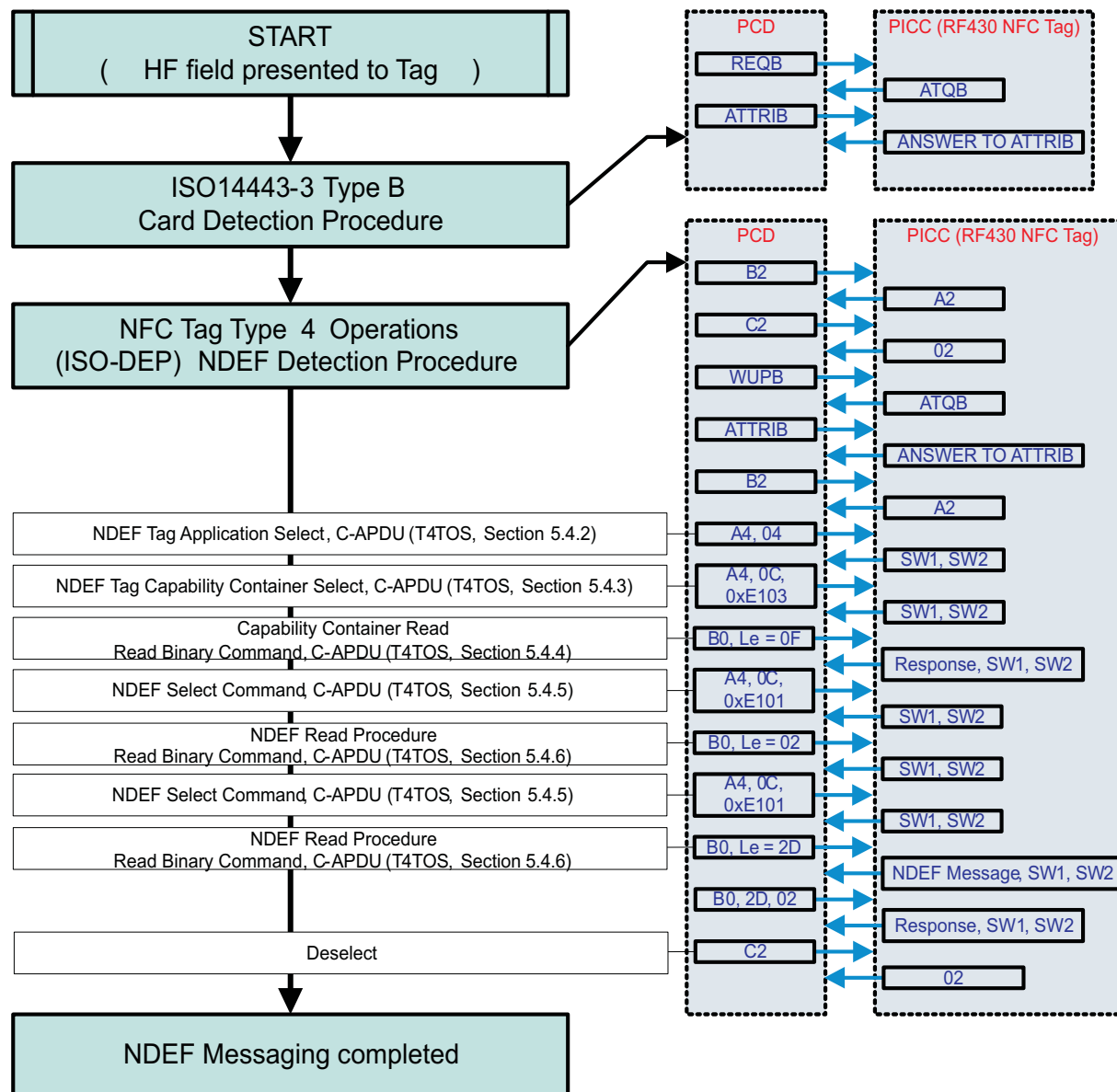


Figure 8. Command and Response Exchange Flow

## **ISO 14443-3 Commands**

These commands use the character, frame format, and timing that are described in ISO 14443-3, clause 7.1. The following commands are used to manage communication:

### **REQB and WUPB**

The REQB and WUPB Commands sent by the PCD are used to probe the field for PICCs of Type B. In addition, WUPB is used to wake up PICCs that are in the HALT state. The number of slots N is included in the command as a parameter to optimize the anticollision algorithm for a given application.

### **Slot-MARKER**

After a REQB or WUPB Command, the PCD may send up to (N-1) Slot-MARKER Commands to define the start of each timeslot. Slot-MARKER Commands can be sent after the end of an ATQB message received by the PCD to mark the start of the next slot or earlier if no ATQB is received (no need to wait until the end of a slot, if this slot is known to be empty).

### **ATTRIB**

The ATTRIB Command sent by the PCD includes information required to select a single PICC. A PICC receiving an ATTRIB Command with its identifier becomes selected and assigned to a dedicated channel. After being selected, this PICC only responds to commands defined in ISO/IEC 14443-4 that include its unique CID.

### **HLTB**

The HLTB Command is used to set a PICC in HALT state and stop responding to a REQB. After answering to this command, the PICC ignores any commands except the WUPB.

## **NFC Tag Type 4 Commands**

### **Select**

Selection of applications or files

### **ReadBinary**

Read data from file

### **UpdateBinary**

Update (erase and write) data to file

## Data Rate Settings

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported by the device.

By default, the device reports only the capability to support 106-kbps, because some cell phones do not work correctly with the information that the device supports higher data rates. To enable higher data rates the sequence shown in [Table 30](#) must be sent through the selected serial interface.

**Table 30. Data Rate Setting Sequence**

Access Type	Addr Bits 15 to 8	Addr Bits 7 to 0	Data 0	Data 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0x78	0xF7 <sup>(1)</sup>	0x00
4. Write Access	0x28	0x14	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to [Table 31](#). 0xF7: all data rates up to 847 kbps are supported.

**Table 31. Data Rate Capability**

Data Rate Capability Byte								Description
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	PICC supports only 106-kbps in both directions (default).
1	x	x	x	0	x	x	x	Same data rate from PCD to PICC and from PICC to PCD compulsory
x	x	x	1	0	x	x	x	PICC to PCD, data rate supported is 212 kbps
x	x	1	x	0	x	x	x	PICC to PCD, data rate supported is 424 kbps
x	1	x	x	0	x	x	x	PICC to PCD, data rate supported is 847 kbps
x	x	x	x	0	x	x	1	PCD to PICC, data rate supported is 212 kbps
x	x	x	x	0	x	1	x	PCD to PICC, data rate supported is 424 kbps
x	x	x	x	0	1	x	x	PCD to PICC, data rate supported is 847 kbps

## NDEF Data Memory

This device implements 3kB of SRAM memory that must be written with the NDEF Application data.

Table 32 shows the mandatory structure. The data can be accessed through the RF interface only after the NDEF application memory is correctly initialized through the serial interface.

While writing into the NDEF application memory, the RF interface must be disabled by clearing the Enable RF bit in the General Control register. After the NDEF application memory is properly initialized, the RF interface can be enabled by setting the Enable RF bit in the General Control register to 1. When the RF interface is enabled, the basic NDEF structure is checked for correctness. If an error in the structure is detected, the NDEF Error IRQ is triggered, and the RF interface remains disabled (the Enable RF bit in the General Control register is cleared to 0).

If the NDEF application data must be modified through the serial interface after the RF interface is enabled, it is recommended to read the RF Busy bit in the Status register. If the RF interface is busy, defer disabling the RF interface until the RF transaction is completed (indicated by RF Busy bit = 0).

Figure 9 shows the recommended flow how to control the access to the NDEF application memory.

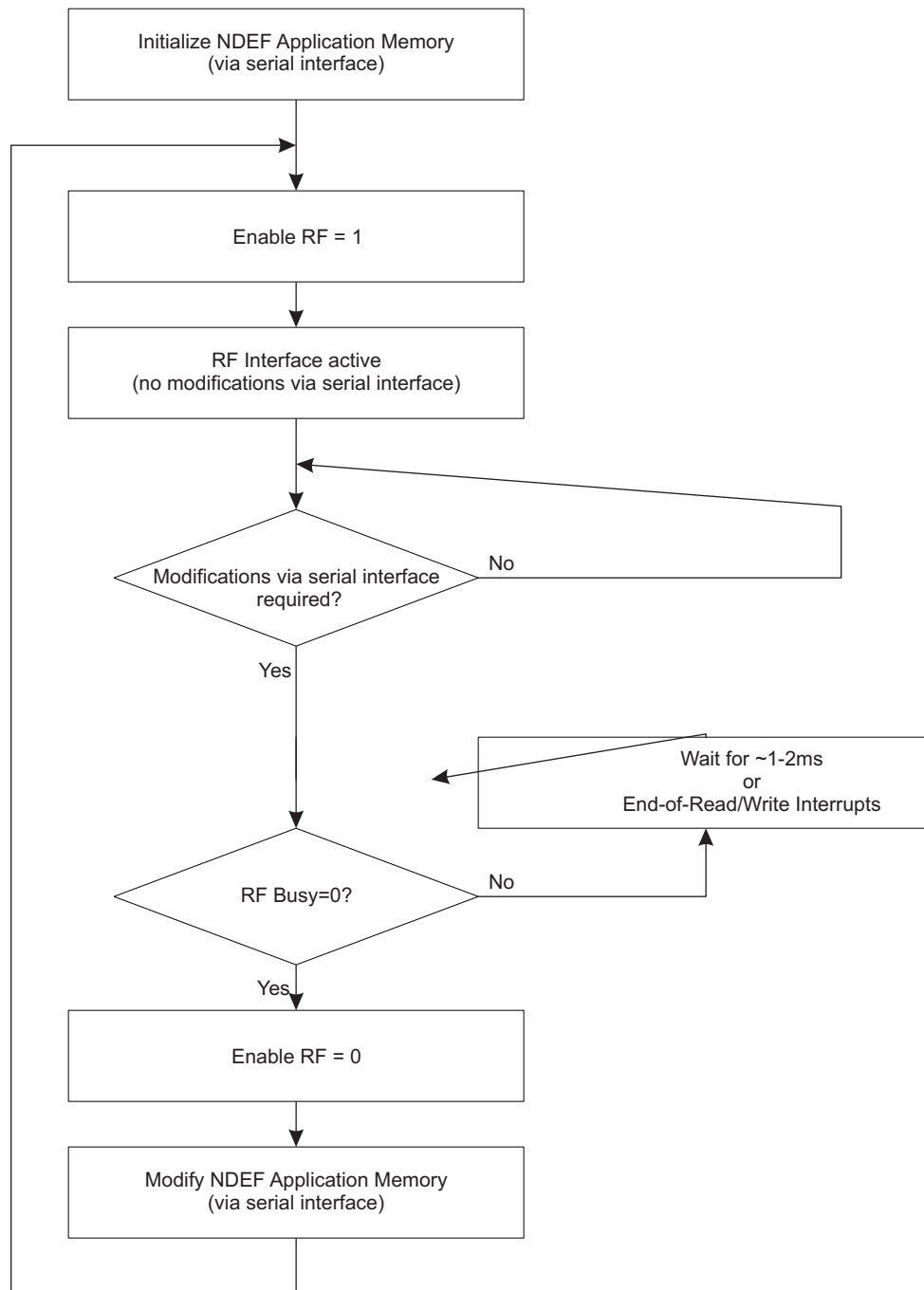
The address range for the NDEF application memory is 0x0000 to 0x0BFF.

**Table 32. NDEF Application Data (Mandatory)**

NDEF Application Selectable by Name = D2_7600_0085_0101h	Capability Container Selectable by File ID = E103h	2B - CCLen		The NDEF file control TLV is mandatory	
		1B - Mapping version			
		2B - MLe			
		2B - MLc			
		NDEF File Ctrl TLV	1B - Tag = 04h		
			1B - Len = 06h		
			6B - Val		2B - File Identifier
	2B - Max file size				
	1B - Read access				
	1B - Write access				
NDEF File Selectable by File ID = xxxyh	2B - Len		Mandatory NDEF file		
	xB - Binary NDEF file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				

**Table 33. NDEF Application Data (Includes Proprietary Sections)**

NDEF Application Selectable by Name = D2_7600_0085_0101h	Capability Container Selectable by File ID = E103h	2B - CCLen			
		1B - Mapping version			
		2B - MLe			
		2B - MLc			
		NDEF File Ctrl TLV	1B - Tag = 04h		The NDEF file control TLV is mandatory
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
		1B - Write access			
		Proprietary File Ctrl TLV (1)	1B - Tag = 05h		Zero or more proprietary file control TLVs
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
	2B - Max file size				
	1B - Read access				
	1B - Write access				
	⋮				
	Proprietary File Ctrl TLV (N)	1B - Tag = 05h			
		1B - Len = 06h			
		6B - Val	2B - File Identifier		
			2B - Max file size		
			1B - Read access		
	1B - Write access				
NDEF File Selectable by File ID = xyyyh	2B - Len		Mandatory NDEF file		
	xB - Binary NDEF file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				
Proprietary File (1) Selectable by File ID = xyyyh	2B - Len		Optional proprietary file		
	xB - Binary proprietary file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				
⋮					
Proprietary File (N) Selectable by File ID = xyyyh	2B - Len		Optional proprietary file		
	xB - Binary proprietary file content				
	yB - Unused if Len < Max file size in File Ctrl TLV				



**Figure 9. Recommended NDEF Data Memory Flow**

## NDEF Error Check

With the RF interface is enabled, the basic NDEF structure is automatically checked for correctness. If any of the following conditions are true, the error check fails, an NDEF error IRQ is triggered, and the RF interface remains disabled.

- CCLen less than 0x000F or greater than 0xFFFFE.
- MLe value is less than 0xF.
- MLc is equal to zero.
- TLV tag does not equal 0x4.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

Also the proprietary TLVs are checked. The check fails if any of the following conditions are true.

- TLV tag does not equal 0x05.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

## Typical Usage Scenario

A typical usage scenario is as follows:

1. Write capability container and messages into the NDEF memory (starting from address 0) using the serial interface.
2. Enable interrupts (especially End of Read and End of Write).
3. Configure the interrupt pin INTO as needed and enable the RF interface.
4. Wait for interrupt signaled by INTO.
5. Disable RF interface (but keep INTO settings unchanged).
6. Read interrupt flag register to determine interrupt sources.
7. Clear interrupt flags. INTO returns to inactive state.
8. Read and modify NDEF memory as needed.
9. Enable RF interface again (keeping INTO settings unchanged) and continue with .

## References

ISO/IEC 14443-1:2000, Part 1: Physical characteristics

ISO/IEC 14443-2: 2001, Part 2: Radio frequency interface power and signal interface

ISO/IEC 14443-3: 2001, Part 3: Initialization and anticollision

ISO/IEC 14443-4: 2001, Part 4: Transmission protocols

ISO/IEC 18092, NFC Communication Interface and Protocol-1 (NFCIP-1)

ISO/IEC 21481, NFC Communication Interface Protocol-2 (NFCIP-2)

NDEF NFC Forum Spec, NFC Data Exchange Format Specification



### Absolute Maximum Ratings<sup>(1)(2)</sup>

Voltage applied at $V_{CC}$ referenced to $V_{SS}$ ( $V_{AMR}$ )	-0.3 V to 4.1 V
Voltage applied at $V_{ANT}$ referenced to $V_{SS}$ ( $V_{AMR}$ )	-0.3 V to 4.1 V
Voltage applied to any pin (references to $V_{SS}$ )	-0.3 V to ( $V_{CC} + 0.3$ V)
Diode current at any device pin	$\pm 2$ mA
Storage temperature range <sup>(3)</sup>	-40°C to 125°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are referenced to  $V_{SS}$ .
- (3) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### Recommended Operating Conditions

Typical values are specified at  $V_{CC} = 3.3$  V and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage during program execution no RF field present	3.0	3.3	3.6	V
	Supply voltage during program execution with RF field present	2.0	3.3	3.6	V
$V_{SS}$	Supply voltage (GND reference)		0		V
$T_A$	Operating free-air temperature	-40		85	°C
$C_{VCC}$	Capacitor on $V_{CC}$ <sup>(1)</sup>		0.1		μF
$C_{V_{CORE}}$	Capacitor on $V_{CORE}$ <sup>(1)</sup>	0.1	0.47	1	μF

- (1) Low ESR (equivalent series resistance) capacitor

### Recommended Operating Conditions, Resonant Circuit

		MIN	NOM	MAX	UNIT
$f_c$	Carrier frequency		13.56		MHz
$V_{ANT\_peak}$	Antenna input voltage			3.6	V
$Z$	Impedance of LC circuit	6.5	15.5		kΩ
$L_{RES}$	Coil inductance		2.66		μH
$C_{RES}$	Resonance capacitance		51.8 – $C_{IN}$ <sup>(1)</sup>		pF
QT	Tank quality factor		20		

- (1) Refer to [RF143B, Recommended Operating Conditions](#).

## Electrical Characteristics

### Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
I <sub>CC(SPI)</sub>	SPI, f <sub>SCK,MAX</sub> , SO = Open, Writing into NDEF memory		3.3 V		250		μA
I <sub>CC(I2C)</sub>	I2C, 400 kHz, Writing into NDEF memory		3.3 V		250		μA
I <sub>CC(RF enabled)</sub>	RF enabled, no RF field present		3.3 V		200		μA
I <sub>CC(Inactive)</sub>	Standby enable = 0, RF disabled, no serial communication		3.3V		40		μA
I <sub>CC(Standby)</sub>	Standby enable = 1, RF disabled, no serial communication		3.3 V		10	45	μA
ΔI <sub>CC(StrongRF)</sub>	Additional current consumption with strong RF field present		3.0 V to 3.6 V			160	μA
I <sub>CC(RF,lowVCC)</sub>	Current drawn from VCC < 3.0 V with RF field present (passive operation)		2.0 V to 3.0 V			0	μA

### Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>IL</sub>	Low-level input voltage					0.3× V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage			0.7× V <sub>CC</sub>			V
V <sub>HYS</sub>	Input hysteresis			0.1× V <sub>CC</sub>			V
I <sub>L</sub>	High-impedance leakage current		3.3 V	-50		50	nA
R <sub>PU(RST)</sub>	Integrated $\overline{\text{RST}}$ pullup resistor			20	35	50	kΩ
R <sub>PU(CS)</sub>	Integrated SCMS/ $\overline{\text{CS}}$ pullup resistor (only active during initialization)			20	35	50	kΩ

### Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 3 mA	3 V			0.4	V
			3.3 V			0.4	
			3.6 V			0.4	
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = -3 mA	3 V	2.6			V
			3.3 V	2.9			
			3.6 V	3.2			

## Serial Communication Protocol Timings

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
t <sub>SP</sub> lvsl2C	Time after power-up or reset until SCMS/ $\overline{\text{CS}}$ is sampled for SPI or I2C decision. <sup>(1)</sup>		1		10	ms
t <sub>Ready</sub>	Time after power-up or reset until device is ready to communicate using SPI or I2C. <sup>(2)</sup>				20	ms

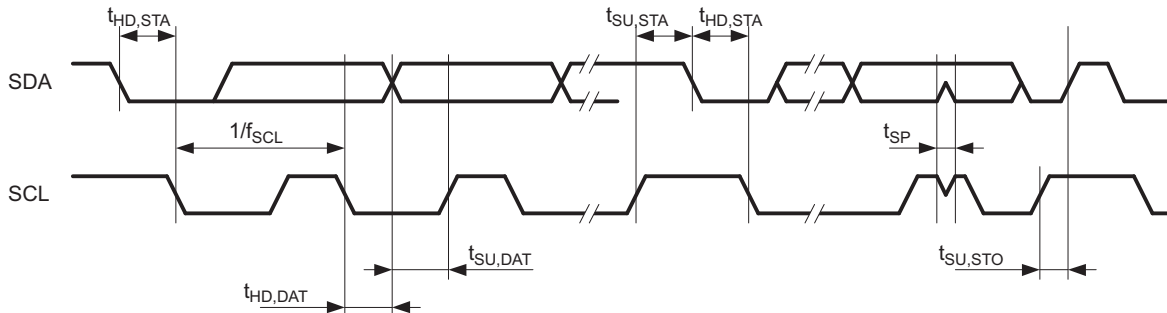
(1) The SCMS/ $\overline{\text{CS}}$  pin is sampled after t<sub>SP</sub>lvsl2C(MIN) at the earliest and after t<sub>SP</sub>lvsl2C(MAX) at the latest.

(2) The device is ready to communicate after t<sub>Ready</sub>(MAX) at the latest.

## I2C Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 10](#))

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>SCL</sub>	SCL clock frequency (with Master supporting clock stretching according to I2C standard, or when the device is not being addressed)	3.3 V	0		400	kHz
	SCL clock frequency (device being addressed by Master not supporting clock stretching)	3.3 V	0		120	kHz
t <sub>HD,STA</sub>	Hold time (repeated) START	3.3 V	4			μs
	f <sub>SCL</sub> ≤ 100 kHz	3.3 V	0.6			μs
t <sub>SU,STA</sub>	Setup time for a repeated START	3.3 V	4.7			μs
	f <sub>SCL</sub> > 100 kHz	3.3 V	0.6			μs
t <sub>HD,DAT</sub>	Data hold time	3.3 V	0			ns
t <sub>SU,DAT</sub>	Data setup time	3.3 V	250			ns
t <sub>SU,STO</sub>	Setup time for STOP	3.3 V	4			μs
t <sub>SP</sub>	Pulse duration of spikes suppressed by input filter	3.3 V	6.25		75	ns



**Figure 10. I2C Mode Timing**

## SPI Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>SCK</sub> SCK clock frequency	write	3.3 V	0		100	kHz
	read	3.3 V	0		110	kHz
t <sub>HIGH,CS</sub> $\overline{\text{CS}}$ high time		3.3 V	50			μs
t <sub>SU,CS</sub> $\overline{\text{CS}}$ setup time		3.3 V	25			μs
t <sub>HD,CS</sub> $\overline{\text{CS}}$ hold time		3.3 V	100			ns
t <sub>HIGH</sub> SCK high time		3.3 V	100			ns
t <sub>LOW</sub> SCK low time		3.3 V	100			ns
t <sub>SU,SI</sub> Data In (SI) setup time		3.3 V	50			ns
t <sub>HD,SI</sub> Data In (SI) hold time		3.3 V	50			ns
t <sub>VALID,SO</sub> Output (SO) valid		3.3 V	0		50	ns
t <sub>HOLD,SO</sub> Output (SO) hold time		3.3 V	0			ns

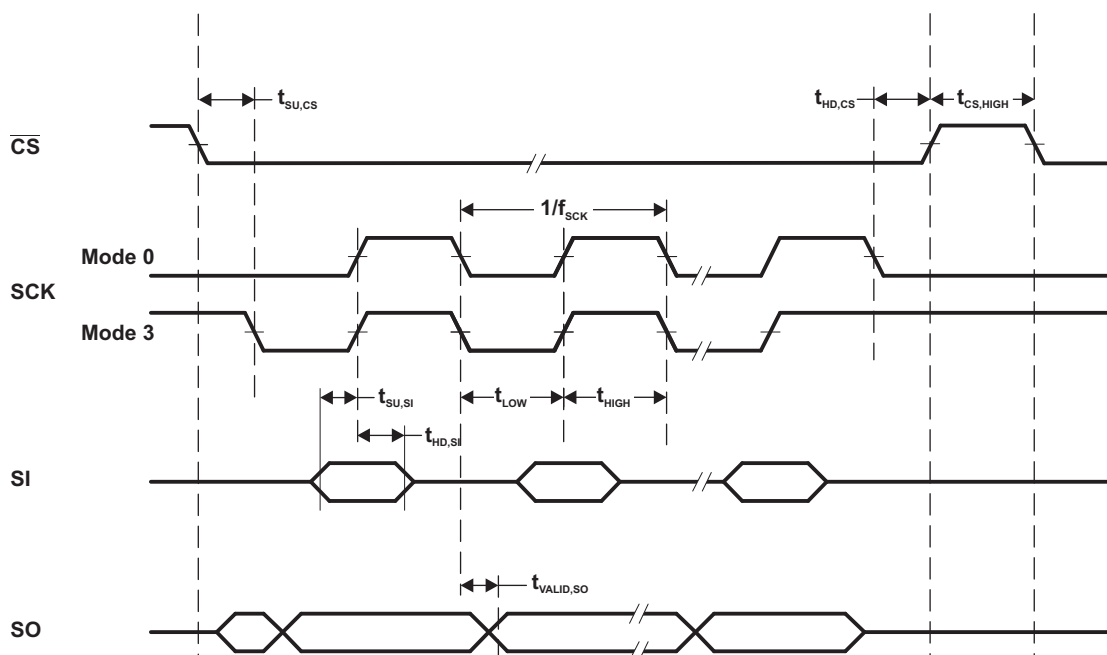


Figure 11. SPI Mode Timing

## RF143B, Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DDH</sub>	Antenna rectified voltage	Peak voltage limited by antenna limiter	3.0	3.3	3.6	V
I <sub>DDH</sub>	Antenna load current	RMS, without limiter current			100	μA
C <sub>IN</sub>	Input capacitance	ANT1 to ANT2, 2 V RMS	31.5	35	38.5	pF

## RF143B, ISO14443B ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DR <sub>10</sub>	Input signal data rate 10% downlink modulation, 7% to 30% ASK, ISO1443B		106	848	kbps
m <sub>10</sub>	Modulation depth 10%, tested as defined in ISO10373	7		30	%

## RF143B, ISO14443B Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f <sub>PICC</sub>	Uplink subcarrier modulation frequency	0.2		1	MHz
V <sub>A_MOD</sub>	Modulated antenna voltage, V <sub>A_unmod</sub> = 2.3 V	0.5			V
V <sub>SUB14</sub>	Uplink modulation subcarrier level, ISO14443B: H = 1.5 to 7.5 A/m	22/H <sup>0.5</sup>			mV

## RF143B, Power Supply

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>LIM</sub>	Limiter clamping voltage	I <sub>LIM</sub> ≤ 70 mA RMS, f = 13.56 MHz	3.0		3.6	V <sub>pk</sub>
I <sub>LIM,MAX</sub>	Maximum limiter current				70	mA

## REVISION HISTORY

REVISION	COMMENTS
SLAS916	Product Preview release
SLAS916A	Production Data release

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RF430CL330HCPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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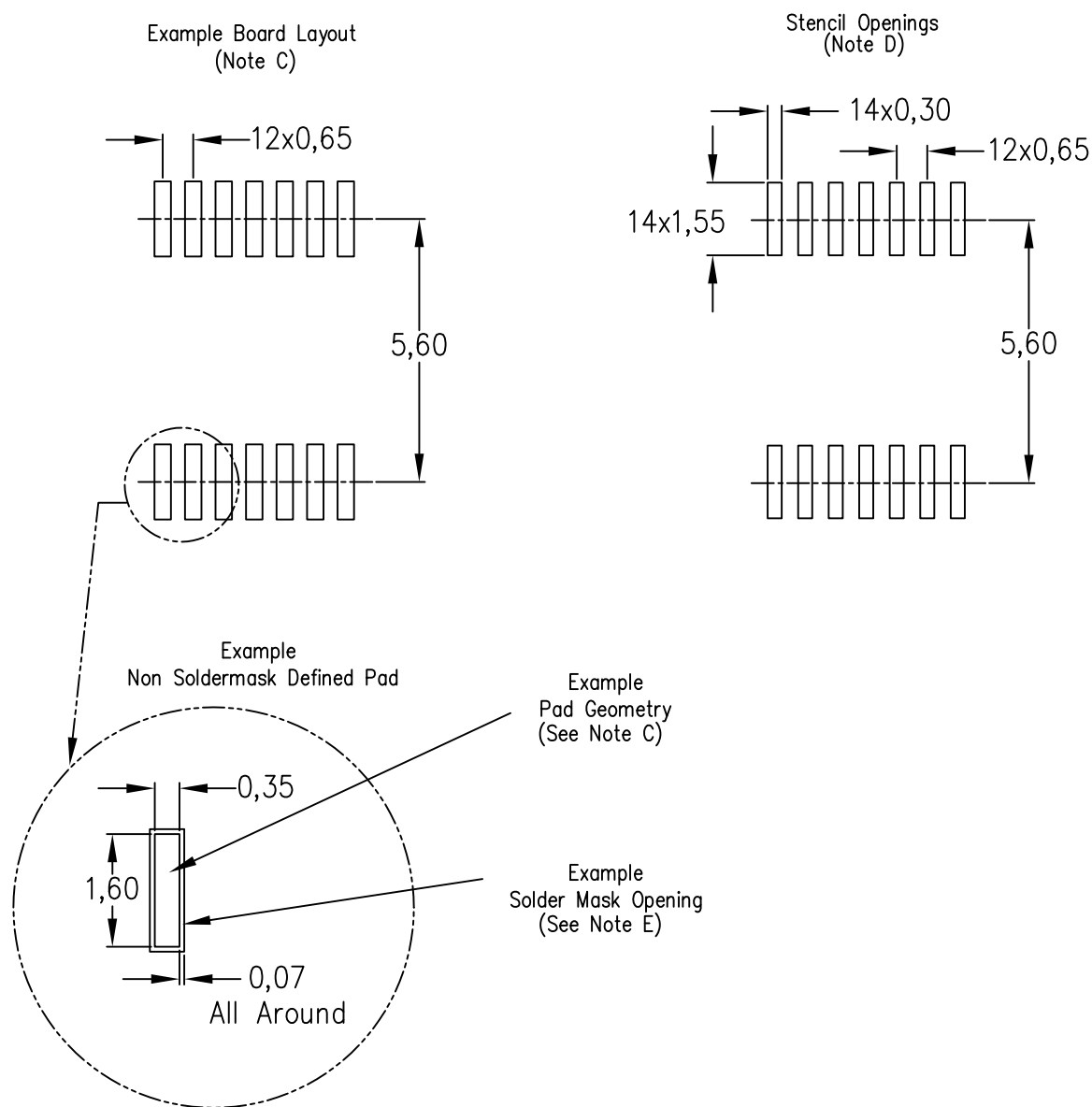
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com.cn/omap">www.ti.com.cn/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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